

## List of Figures

Figure 1-1	Directed test progress over time	6
Figure 1-2	Directed test coverage	7
Figure 1-3	Constrained-random test progress over time vs. directed testing	8
Figure 1-4	Constrained-random test coverage	9
Figure 1-5	Coverage convergence	9
Figure 1-6	Test progress with and without feedback	13
Figure 1-7	The testbench — design environment	14
Figure 1-8	Testbench components	15
Figure 1-9	Signal and command layers	18
Figure 1-10	Testbench with functional layer added	18
Figure 1-11	Testbench with scenario layer added	19
Figure 1-12	Full testbench with all layers	20
Figure 1-13	Connections for the driver	21
Figure 2-1	Unpacked array storage	31
Figure 2-2	Packed array layout	35
Figure 2-3	Packed array bit layout	36
Figure 2-4	Associative array	41
Figure 4-1	The testbench – design environment	89
Figure 4-2	Testbench – Arbiter without interfaces	91
Figure 4-3	An interface straddles two modules	93
Figure 4-4	Main regions inside a SystemVerilog time step	104
Figure 4-5	A clocking block synchronizes the DUT and testbench	106
Figure 4-6	Sampling a synchronous interface	108
Figure 4-7	Driving a synchronous interface	110
Figure 4-8	Testbench – ATM router diagram without interfaces	121
Figure 4-9	Testbench - router diagram with interfaces	125
Figure 5-1	Handles and objects after allocating multiple objects	140
Figure 5-2	Static variables in a class	146
Figure 5-3	Contained objectsSample 5-22	151
Figure 5-4	Handles and objects across methods	155
Figure 5-5	Objects and handles before copy with the new operator	159

Figure 5-6	Objects and handles after copy with the new operator	160
Figure 5-7	Objects and handles after copy with the new operator	160
Figure 5-8	Objects and handles after deep copy	162
Figure 5-9	Layered testbench	165
Figure 6-1	Building a bathtub distribution	196
Figure 6-2	Random strobe waveforms	206
Figure 6-3	Sharing a single random generator	220
Figure 6-4	First generator uses additional values	220
Figure 6-5	Separate random generators per object	221
Figure 7-1	Testbench environment blocks	232
Figure 7-2	Fork...join blocks	233
Figure 7-3	Fork...join block	234
Figure 7-4	Fork...join block diagram	244
Figure 7-5	A mailbox connecting two transactors	254
Figure 7-6	A mailbox with multiple handles to one object	256
Figure 7-7	A mailbox with multiple handles to multiple objects	256
Figure 7-8	Layered testbench with environment	267
Figure 8-1	Simplified layered testbench	276
Figure 8-2	Base Transaction class diagram	277
Figure 8-3	Extended Transaction class diagram	278
Figure 8-4	Blueprint pattern generator	282
Figure 8-5	Blueprint generator with new pattern	282
Figure 8-6	Simplified extended transaction	287
Figure 8-7	Multiple inheritance problem	294
Figure 8-8	Callback flow	299
Figure 9-1	Coverage convergence	326
Figure 9-2	Coverage flow	327
Figure 9-3	Bug rate during a project	330
Figure 9-4	Coverage comparison	332
Figure 9-5	Uneven probability for packet length	361
Figure 9-6	Even probability for packet length with solve...before	361
Figure 10-1	Router and testbench with interfaces	368
Figure 11-1	The testbench – design environment	388
Figure 11-2	Block diagram for the squat design	388
Figure 12-1	Storage of a 40-bit 2-state variable	428
Figure 12-2	Storage of a 40-bit 4-state variable	429